PT4201

Current-mode PWM Controller

GENERAL DESCRIPTION

PT4201 is a highly integrated current mode PWM controller， providing low standby power and cost effective system solution for the sub 30W flyback converter applications. It is also suitable for high precision and high reliable LED lighting applications.

It features power saving operation at no load or light load condition, PWM frequency is reduced to minimize switching loss and low standby power and high efficiency is thus achieved. PT4201 also features low VDD startup current which also contributes to low standby power. The built in LEB on the current sense input removes the signal glitch due to snubber circuit diode reverse recovery thus reduce the external component count and system cost in the design.

Rich protection is implemented in PT4201 including cycle-by-cycle current limiting (OCP), over load protection (OLP), VDD over voltage clamp and under voltage lockout (UVLO). Gate drive output is clamped at 18V to protect the power MOSFET. By limiting the minimum frequency above 22 kHz eliminates the potential audible noise when the system works under light or no load conditions.

Excellent EMI performance is achieved with C.R.PowTech proprietary frequency Jittering technique together with soft driving control at totem pole gate drive output.

The PT4201 is available in SOT23-6, SOP-8 and DIP-8 packages.

FEATURES

- Frequency Jittering for Improved EMI Performance
- Green-Mode PWM for Improved Efficiency and Minimum standby power design
- Low start up current 20uA (Typ. 3uA) and Low operation current 2mA (Typ. 1mA)
- Current mode operation
- Leading-edge blanking on current sense input
- Programmable PWM frequency
- Constant output power limit for universal AC input
- Built-in power limit control (OLP)
- Cycle-by-cycle current limiting (OCP)
- Under voltage lockout (UVLO)
- GATE output maximum voltage clamped at 18V
- Totem pole output includes soft driving for better EMI

APPLICATIONS

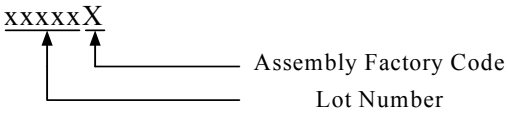
Offline AC/DC flyback converter for

- Power Adapter
- Open-frame SMPS
- Battery Charger Adapter
- 1W-30W HB LED lighting.

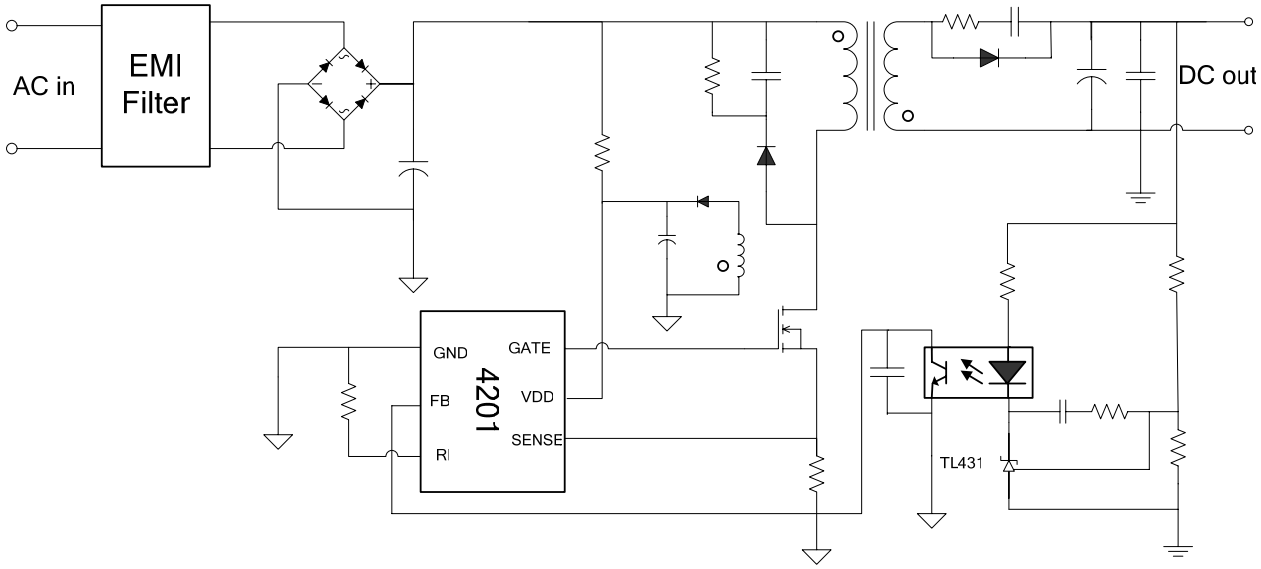
ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDERING PART NUMBER	TRANSPORT MEDIA	MARKING
SOT23-6, Pb free	-40℃ to 85℃	PT4201E23F	Tape and Reel	4201
DIP8, Pb free	-40℃ to 85℃	PT4201EDIH	Tube	PT4201 xxxxxX
SOP8, Pb free	-40℃ to 85℃	PT4201ESOH	Tape and Reel	PT4201 xxxxxX

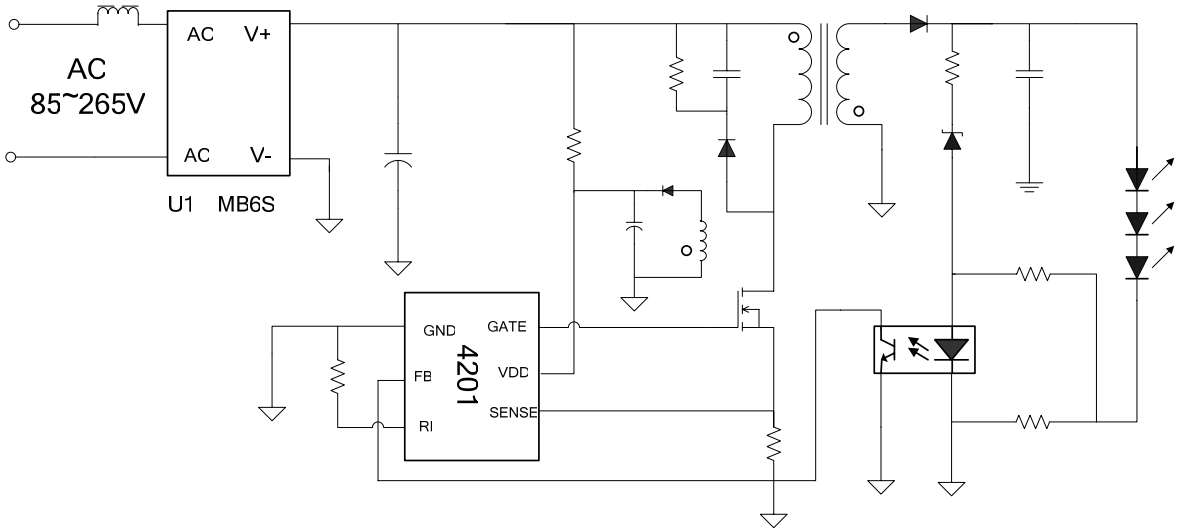
Note:



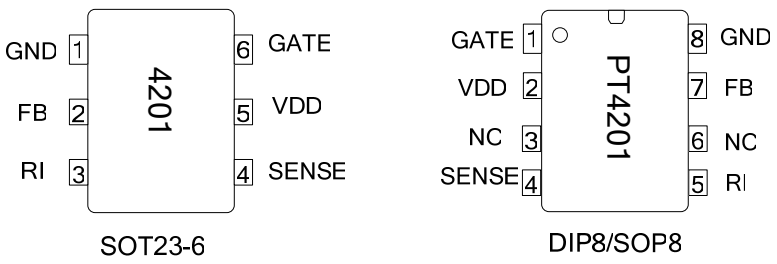
TYPICAL APPLICATIONS (Switching Power Supply)



TYPICAL APPLICATIONS (HB LED Lighting)



PIN ASSIGNMENT



PIN DESCRIPTIONS

NAMES	PIN No. (SOT23-6)	PIN No. (SOP8, DIP8)	DESCRIPTION
GND	1	8	Ground
FB	2	7	Feedback input pin. PWM duty cycle is determined by voltage level into this pin and SENSE pin voltage level.
RI	3	5	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
SENSE	4	4	Current sense input pin. Connected to MOSFET current sensing resistor node.
VDD	5	2	DC power supply pin.
GATE	6	1	Totem-pole gate drive output for power MOSFET.
		3, 6	No Connection

ABSOLUTE MAXIMUM RATINGS (note1)

SYM	PARAMETER	VALUE	UNIT
V_{DD}	V_{DD} DC Supply Voltage	30	V
V_{Clamp}	V_{DD} Clamp Voltage	33	V
$I_{DD\ -Clamp}$	V_{DD} DC Clamp Current	10	mA
V_{FB}	V_{FB} PIN Input Voltage	-0.3~7	V
V_{SENSE}	V_{SENSE} Input Voltage	-0.3~7	V
V_{RI}	V_{RI} Input Voltage	-0.3~7	V
T_J	Min/Max Operating Junction Temperature T_J	-40~150	℃
T_{STG}	Storage Temperature Range	-55~160	℃
HBM	ESD Capability, HBM model(note 2)	2.0	KV

PACKAGE DISSIPATION RATING

SYM	PARAMETER	VALUE	UNIT
$R_{\Theta JA}$	DIP8	90	℃/W
	SOP8	150	℃/W
	SOT23-6	250	℃/W

OPERATING RANGE

SYM	PARAMETER	VALUE	UNIT
V_{DD}	V_{DD} Supply Voltage	10~30	V
RI	RI Resistor Value	100	Kohm
T_A	Operating Ambient Temperature	-20~85	℃

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Range indicates conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Range. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: Human body model, 100pF discharged through a 1.5kΩ resistor.

ELECTRICAL CHARACTERISTICS

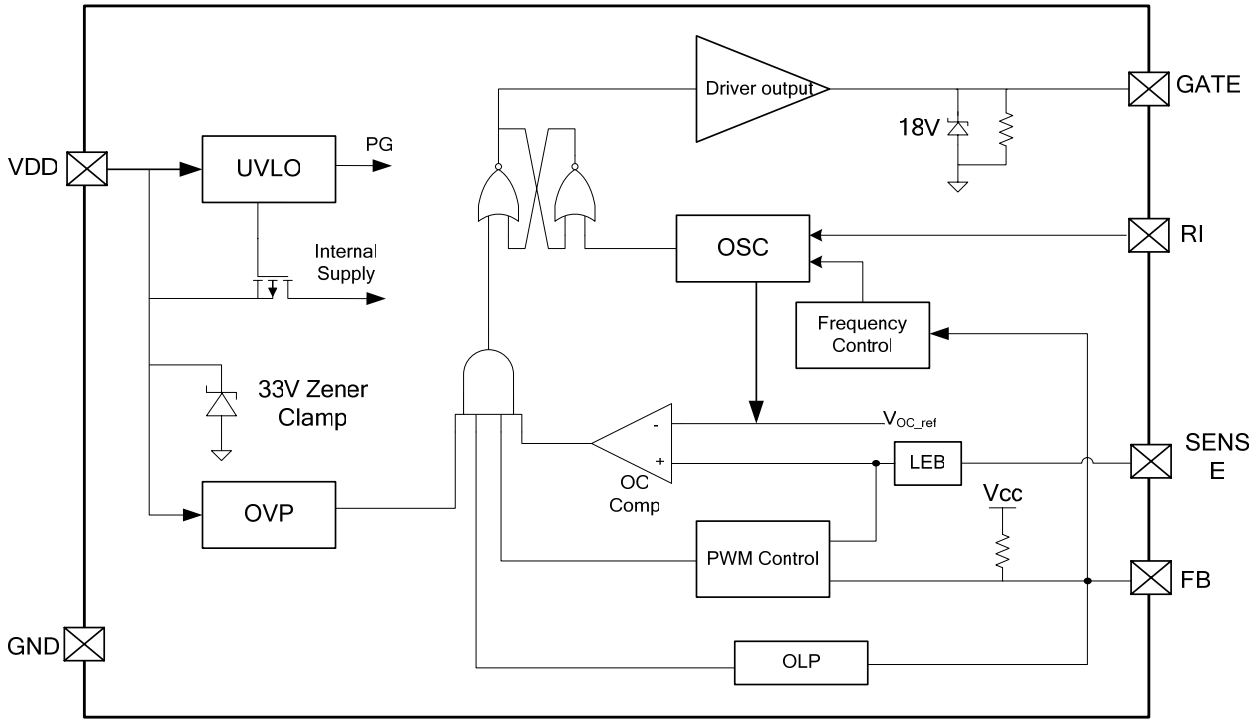
(T_{OPT}=25℃, VDD=16V，unless specified otherwise)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VDD)						
V_{DD_ON}	V_{DD} Start-up voltage	V_{DD} rising	14.0	15.0	16.0	V
V_{DD_MIN}	V_{DD} minimum operating level	V_{DD} falling	6.5	7.5	8.5	V
V_{DD_OVP}	V_{DD} Over Voltage Protection Level	V_{DD} rising	22.5	24.0	25.5	V
$V_{DD\_OVP\_OFF}$	V_{DD} Over Voltage Protection Release Level	V_{DD} falling	21.0	22.5	24.0	V
V_{OVP_HYS}	V_{DD} Over Voltage Hysteresis	V_{DD_OVP}-$V_{DD\_OVP\_OFF}$		1.5		V
V_{ZENER}	V_{DD} Pin Zener Diode Clamp Voltage	I(V_{DD})=5mA		33		V
Current Into VDD						
I_{VDD_START}	V_{DD} Start-up Current	V_{DD}=13.5V Measuring Current into V_{DD}		3	20	uA
I_{VDD_OPER}	V_{DD} Operating Current	V_{DD}=16V, RI=100Kohm V_{FB}=3V, Gate Floating		1		mA
FEED BACK PIN (FB)						
V_{OFB}	V_{FB} Open Loop Voltage	V_{DD}=16V,		4.8		V
V_{PL}	FB Over Load Protection level			3.7		V
V_{GM}	Green Mode FB Threshold			1.6		V
V_{BM}	Burst Mode Entering Threshold			1.2		V
V_{ZD}	Zero Duty Cycle FB Threshold	V_{DD}=16V, RI=100Kohm			0.70	V
T_{PL_DELAY}	Over Load Protection Delay Time	RI=100Kohm		32		ms
Z_{FB}	FB Pin Input Impendence			6.0		Kohm
I_{FB}	FB Pin Supply Current	FB Short To GND, Measuring Current Flowing From FB Pin		0.8		mA
OSCILLATOR (OSC)						
F_{osc}	Oscillator Frequency	RI=100Kohm	60	65	70	kHz
$\triangle F_{JIT}$	△Fosc/Fosc	RI=100Kohm	-3		3	%
$T_{JITTRING}$	Frequency Modulation Period	RI=100Kohm		32		mS
F_{MIN}	Minimum PWM Frequency	V_{DD}=16V, RI=100Kohm		22		kHz
RI	Acceptable RI Range		50	100	250	Kohm

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
F_{DT}	Oscillator Frequency Stability At Different Temperature	V_{DD}=16V, RI=100Kohm -20°C 到 100°C		2		%
F_{DV}	Oscillator Frequency Stability At Different VDD Input Level	V_{DD}=12~25V, RI=100Kohm		2		%
PWM SECTION						
A_V	PWM Input GAIN	$\triangle V_{FB}/\triangle V_{CS}$		2.0		V/V
T_{BLK}	Leading Edge Blanking Time			300		ns
D_{MAX}	PWM Maximum Duty Cycle			75		%
D_{MIN}	PWM Minimum Duty Cycle				0	%
CURRENT SENSE INPUT (SENSE)						
Z_{CS}	SENSE Input Impendence			80		Kohm
V_{TH_OC}	OCP Threshold at Duty=0	FB=3V, V_{GATE}<0.3V	0.70	0.75	0.80	V
T_{OC_DELAY}	Delay Time From OCP to Gate Output OFF	V_{DD}=16V, CS>V_{TH_OC} , C_{GATE}=1000pF		100		nS
GATE OUTPUT						
V_{OL}	GATE Output Low Level	V_{DD}=16V, Io=-20mA			0.8	V
V_{OH}	GATE Output High Level	V_{DD}=16V, Io=20mA	10			V
T_r	GATE Output Rising time	V_{DD}=16V, CL=1000pF		220		nS
T_f	GATE Output Falling Time	V_{DD}=16V, CL=1000pF		70		nS
V_{GMAX}	GATE Output Clamp Voltage			18		V

SIMPLIFIED BLOCK DIAGRAM



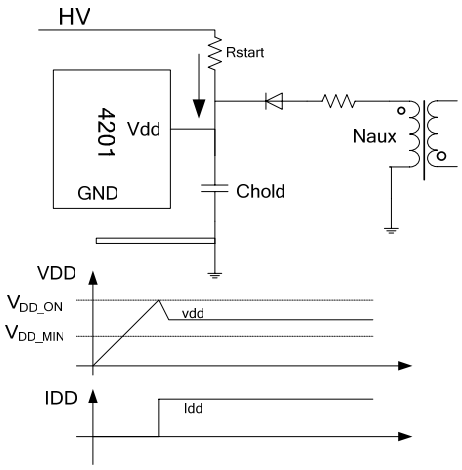
OPERATION DESCRIPTION

With enhanced functions and extremely low start up current and low operating current together with optimized controlling mode, the PT4201 is easy to meet the high performance as well as low standby power requirement in the SMPS application. Its detail features are described as below:

STARTUP AND UVLO:

The start up of PT4201 is realized through the current provided by a resistor connecting to HV line charges the capacitor connecting to VDD pin to the start up threshold voltage. As shown below, initially the voltage on Chold is below the start up threshold the PT4201 stays in UVLO status. The current supplied by Rstart charges the Chold thus the voltage on VDD increases. The PT4201 starts to operate when the voltage on VDD reaches V_{DD_ON} start up threshold. After startup the PT4201 begins to deliver drive signal on GATE and the operating current is supplied by the auxiliary winding of the transformer.

Since the PT4201 sinks a few macro amperes of current before start up, a large start up resistor could be used in the start up circuit to minimize standby power. As for the applications with general AC input range a 2Mohm 1/8W resistor and a 10uF/50V capacitor compose a simple and reliable start up circuit.

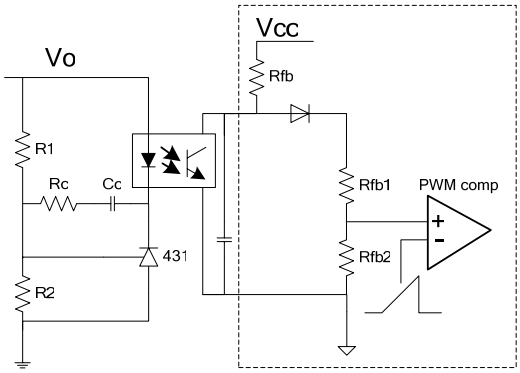


OPERATING CURRENT：

The PT4201 is fabricated with BiCMOS process, the operating current has been reduced to less 1mA when GATE is floating, thus the system efficiency is improved and at the same time, a smaller hold up capacitor can be used to speed up start up progress.

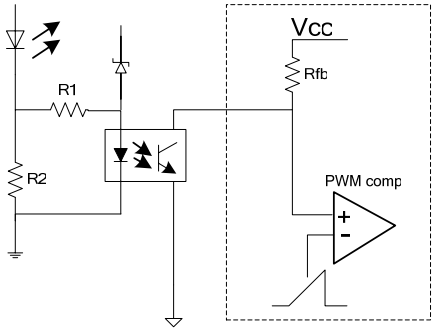
FEEDBACK AND PWM （SMPS application）：

The PT4201 adopts current mode control scheme. the voltage feedback loop is closed by the TL431 and an opto-coupler connected between output node and FB pin, as shown below: A 2.5V reference voltage has been implemented in the TL431, if the divided voltage of R1 and R2 is less than 2.5V TL431 sinks current from Vo and the current is transferred to the FB pin by the opto-coupler. The transferred current is loaded by a resistor connected to the internal regulator output so FB pin voltage is determined and thus PWM signal is generated.



CONSTANT CURRENT OPERATION （LED application）：

PT4201 senses the LED current via an opto-coupler and generates a PWM driving signal to control the LED current. Reference to the following schematic, current sense resistor R2 and turn on voltage of the opto-coupler determine the LED current. When the voltage across R2 turns the opto-coupler on the current of the photo diode of the opto-coupler drives FB PIN decrease so the duty cycle of PWM signal is decreased thus the output current is limited. So the output current can be calculated as Iout=Vonopto/R2. Vonopto represents the LED turn on voltage of the opto-coupler.



ENERGY SAVE OPERATION AT LIGHT LOAD:

Generally the SMPS switching loss is proportional to switching frequency of power MOSFET. In order to achieve high conversion efficiency when the load decrease PT4201 automatically debase PWM frequency to reduce switching loss. The reduction of the load current results in the decrease of voltage on FB pin, when the voltage on FB pin is lower than 1.6V the PWM frequency will linearly decrease with V_{FB} until touch bottom which is 1/3 normal operating frequency. If the FB pin voltage drops below the preset level the PT4201 enters burst mode operation, some PWM cycles is skipped to minimize switching loss. Moreover if the FB pin voltage falls below Zero-Duty level the PWM is disabled immediately until it recovers to above Zero-Duty threshold.

LED OPEN CIRCUIT (LED application)：

When LED open circuit occurs, the output voltage rises to break down the zener diode. The inverse current of the zener diode generates a voltage across R1 and R2 to turn on the opto-coupler, thus the voltage on FB pin decrease to reduce the PWM signal duty cycle, so that the power delivered to the output is limited. Therefore the system is safe under LED open circuit condition.

LED SHORT CIRCUIT (LED application)：

When LED short circuit occurs, for the output voltage is low and the output current is limited thus the output power is so small that the system is safe. Because the voltage on auxiliary winding is proportion to the output voltage, VDD will then drops due to internal power consumption. When VDD drops below the V_{DD_MIN} turn-off threshold, the PT4201 will be totally shut down. When this happens, the start up sequence will kick in and VDD is charging up again. when the current sense

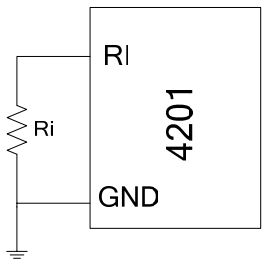
resistor is shorted, because the opto-coupler is turned off the voltage on FB will rise over the protection threshold which is set to be 3.7V, after a delay time the PT4201 will stop delivering PWM signal to protect the system from being damaged.

OSCILLATOR AND FREQUENCY JITTERING:

The operating frequency can be easily set via a resistor connected to the RI pin and GND. The relationship between operating frequency and RI follows the expression: Fosc=6500/RI. Which Fosc represents normal operating frequency with unit in KHz, and RI with unit in Kohm.

The frequency jittering is implemented in the PT4201. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore reduces system design challenge.

Care should be considered that the PWM frequency will be reduced to one third of normal operating frequency so a large RI is not recommended because the audible noise maybe exists when the load is too light.

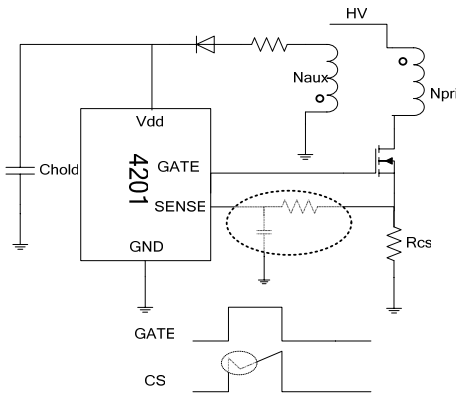


CURRENT SENSE AND LEB:

One function of the SENSE pin is sensing the current of the power MOSFET to generate a current slope and the other function is providing cycle by cycle current limit. The current of the power MOSFET is transferred to voltage signal through a resistor connected between source terminal and GND and feed to SENSE input. The voltage on SENSE and FB determines duty cycle of the PWM signal.

As for cycle by cycle current limit, at each PWM cycle when the voltage of SENSE input excess the internal threshold the PWM signal is terminated after a short delay to protect the power MOSFET. The relationship between the OCP threshold and the current of power MOSFET follows below expression: I_{OC}=Voc/Rcs; Ioc is the current of power MOSFET, Voc is the threshold of OCP and Rcs represents sensing resistor. The internal OCP threshold is modulated by the PWM duty cycle, with zero PWM duty cycle the threshold is 0.75V.

A spike is inevitable on the sensed signal on Rcs at the instance when the power MOSFET is turned on due to the recovery time of the secondary rectifier and the snubber circuit. The LEB has been implemented in PT4201, during the LEB time the OCP comparator is disabled so the PWM signal can not be terminated by the turn-on spike on the sensed signal so the external RC filter can be removed.



INTERNAL SLOPE COMPENSATION:

To eliminate the potential sub-harmonic oscillation problem when the duty cycle excess 0.5, the slope compensation has been implemented in the PT4201. At each PWM duty cycle a constant slope is added to the sensed current ramp so that the system stability is improved.

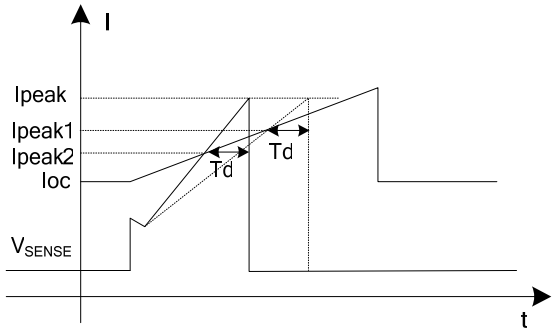
UNIVERSAL INPUT OCP COMPENSATION:

Because there is always a constant delay time Td from OCP is triggered to the power MOSFET is turned off, the actual current of the MOSFET at the instance it is turned off is different from the setting value. Taking the below figure as reference, considering the delay time of Td the actual current is: Ipeak=Ipeak1+Islope1*Td. Islope1=Vindc/Lpri. With a higher input level the actual OCP current is Ipeak=Ipeak2+Islope2*Td, Islope2=Vindc2/Lpri. Which Lpri represents primary winding inductance of transformer; Td is a constant delay time and does not vary with Vin. From above

equations it can be derived that the actual OCP threshold of the power MOSFET is always larger than setting value due to the OCP delay time and the difference increases with the increase of Vin. In order to compensate the difference OCP threshold in PT4201 has been designed to vary with the duty cycle, it means that a smaller duty cycle results in a smaller OCP threshold. When the input AC voltage increase the duty cycle gets small and the OCP point decrease, thus the actual OCP threshold of power MOSFET maintains unchanged in the universal input range. The relationship between OCP threshold voltage and PWM signal duty cycle follows below expression:

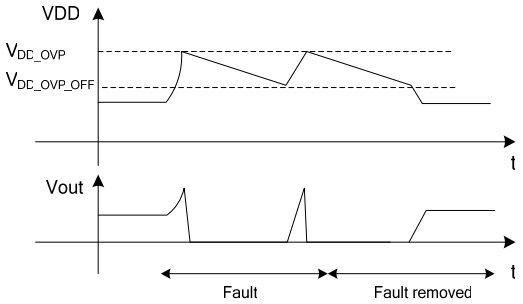
$$Voc=0.75+0.52*Duty$$

Duty represents the duty cycle of PWM signal.



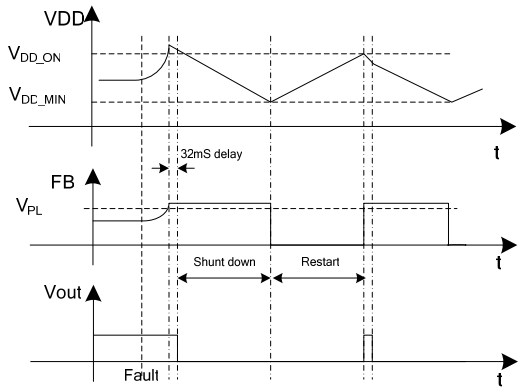
VDD OVER VOLTAGE PROTECTION:

When open loop occurs the opto-coupler does not sink current thus the voltage on FB rise and current limit will be triggered. If the load is not large enough the output voltage will increase because of redundant power is delivered to the load. Under this condition if the OLP is not triggered the output voltage will lost control and the load is in danger of damaged of over voltage. Because the voltage on auxiliary winding is proportional to the output voltage the VDD rises with the output. When the voltage on VDD reaches the OVP threshold the PT4201 stops delivering PWM signal to the power MOSFET, voltage on VDD begins to drop due to the internal power consumption, the PT4201 will recover from OVP status when voltage on VDD drops below the OVP release threshold. The OVP cycle will repeat after recovery until if the fault condition is removed.



OVER LOAD PROTECTION:

The Over Load Protection function (OLP) provides another protection to the system from damage when load short circuit or over load occurs. In that condition the voltage on the FB rise, when the V_{FB} excesses 3.7V the PT4201 starts a timer, after a delay time T_{PL_DELAY} if the fault condition still exists the PWM signal is blocked. VDD will then drops due to internal power consumption. When VDD drops below the V_{DD_MIN} threshold, the PT4201 will be totally shut down. When this happens, the start up sequence will kick in and VDD is charging up again.

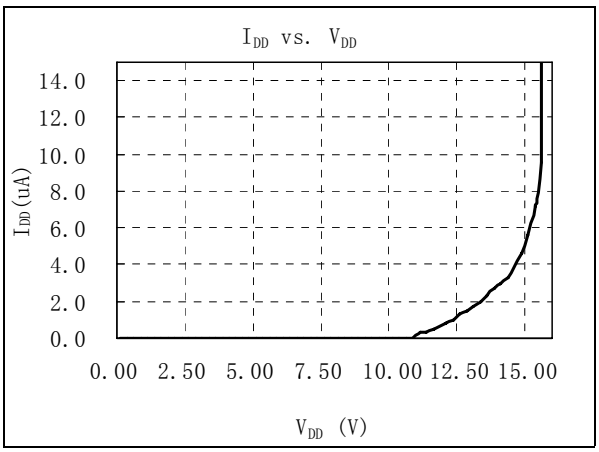


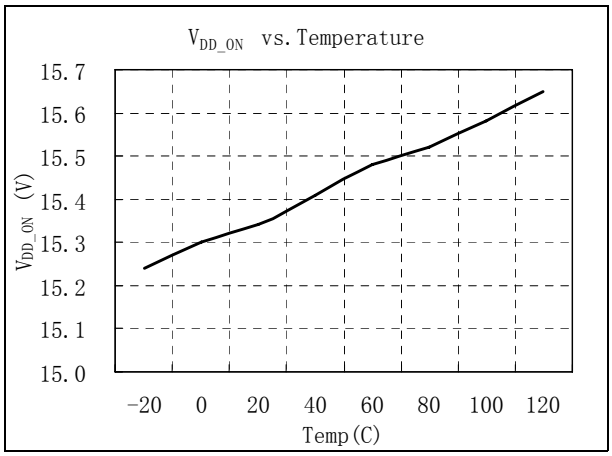
GATE OUTPUT:

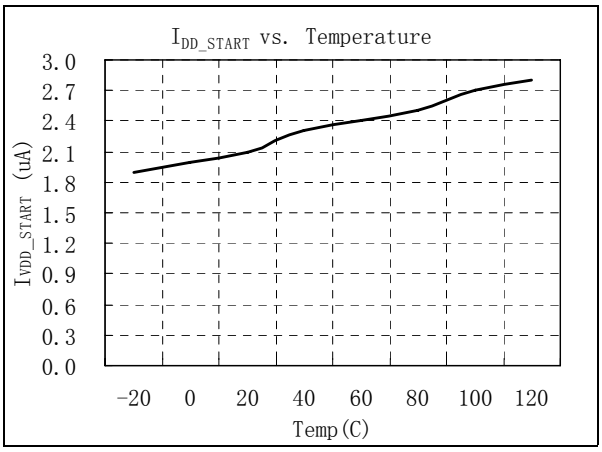
The output drives the GATE of the power MOSFET. The optimized totem-pole type driver offers a good tradeoff between driving ability and EMI. Additionally the output high level is clamped to 18V by an internal clamp so that power MOSFET transistor can be protected against undesirable gate over voltage. A resistor between GATE and GND initials the gate voltage to zero at the off state.

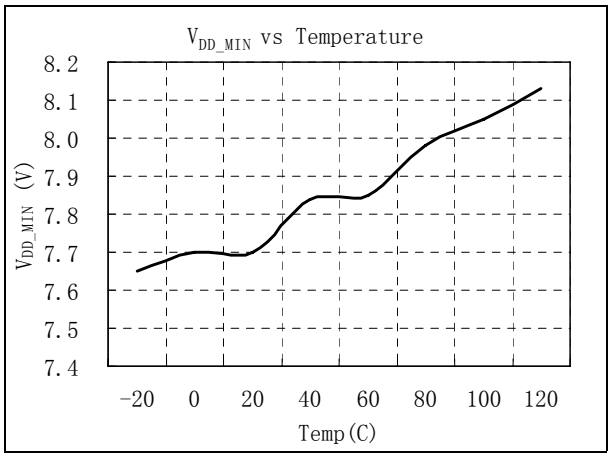
TYPICAL PERFORMANCE CHARACTERISTICS

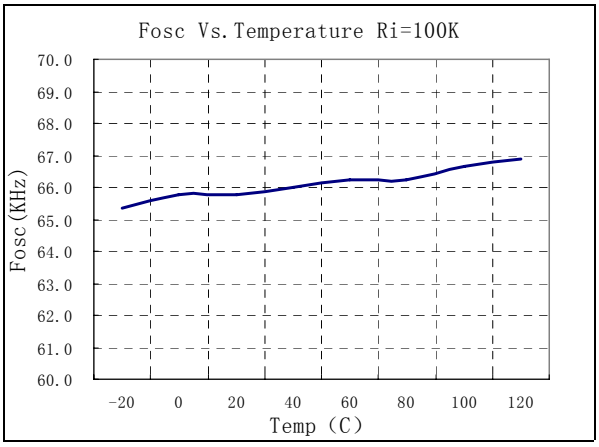
V_{DD}=16V, RI=100Kohm, T_A=25℃ if not otherwise noted

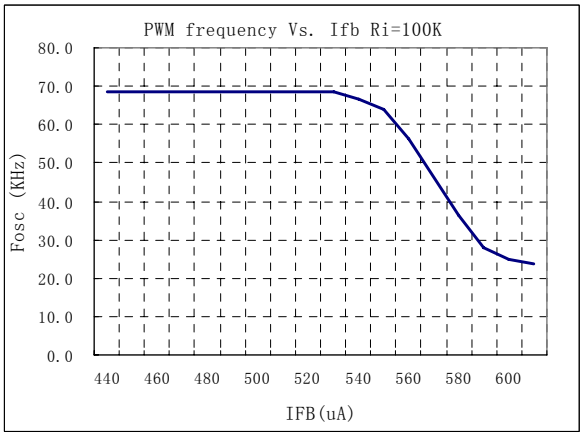




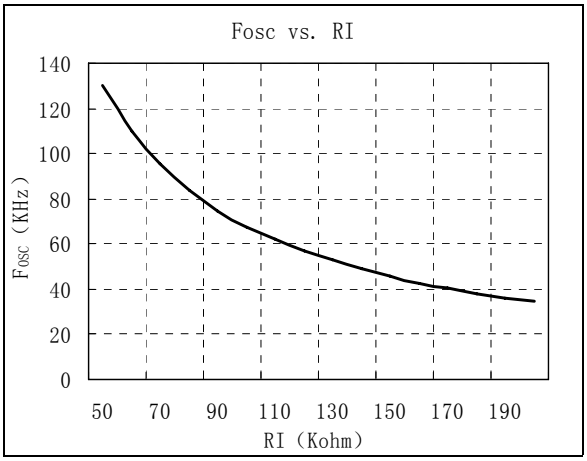


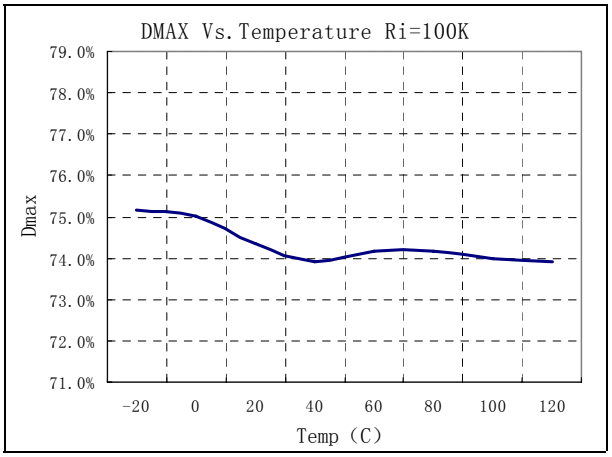


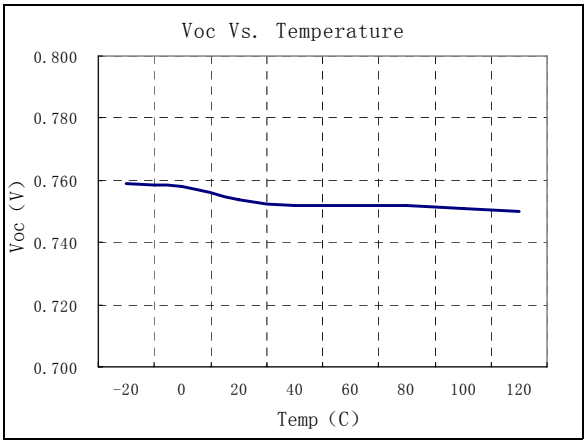


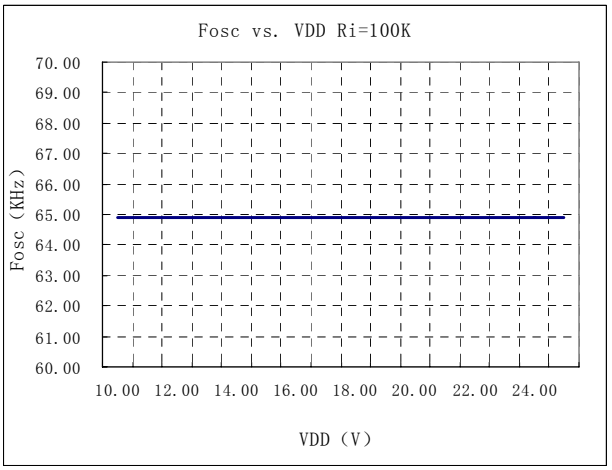


TYPICAL PERFORMANCE CHARACTERISTICS (continued)



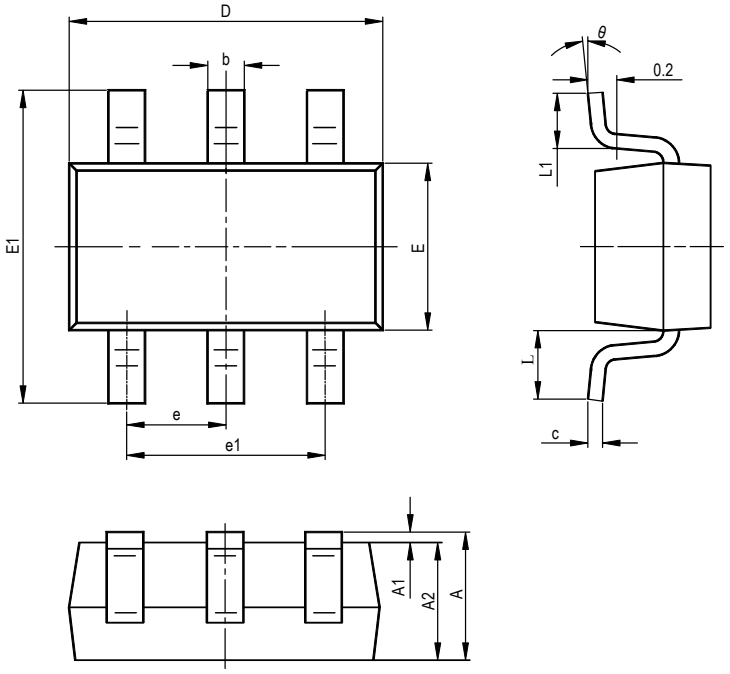






PACKAGE INFORMATION

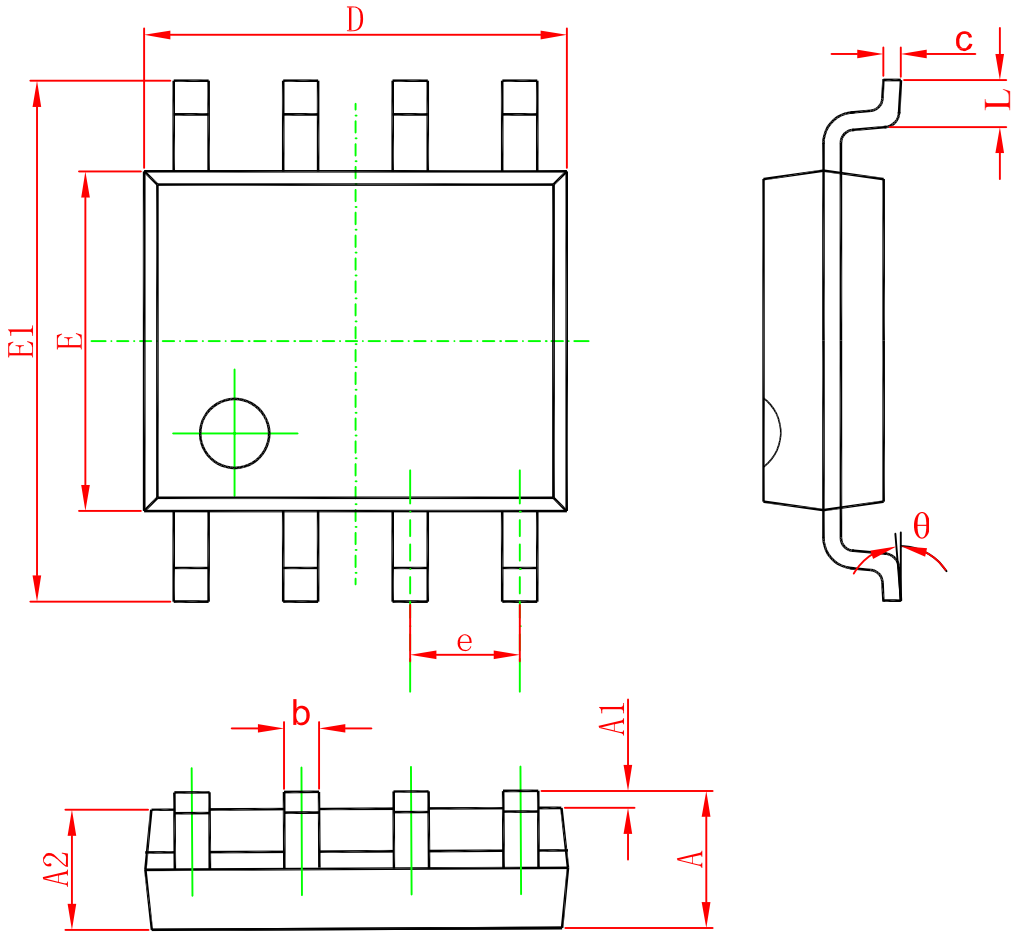
SOT23-6



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

PACKAGE INFORMATION

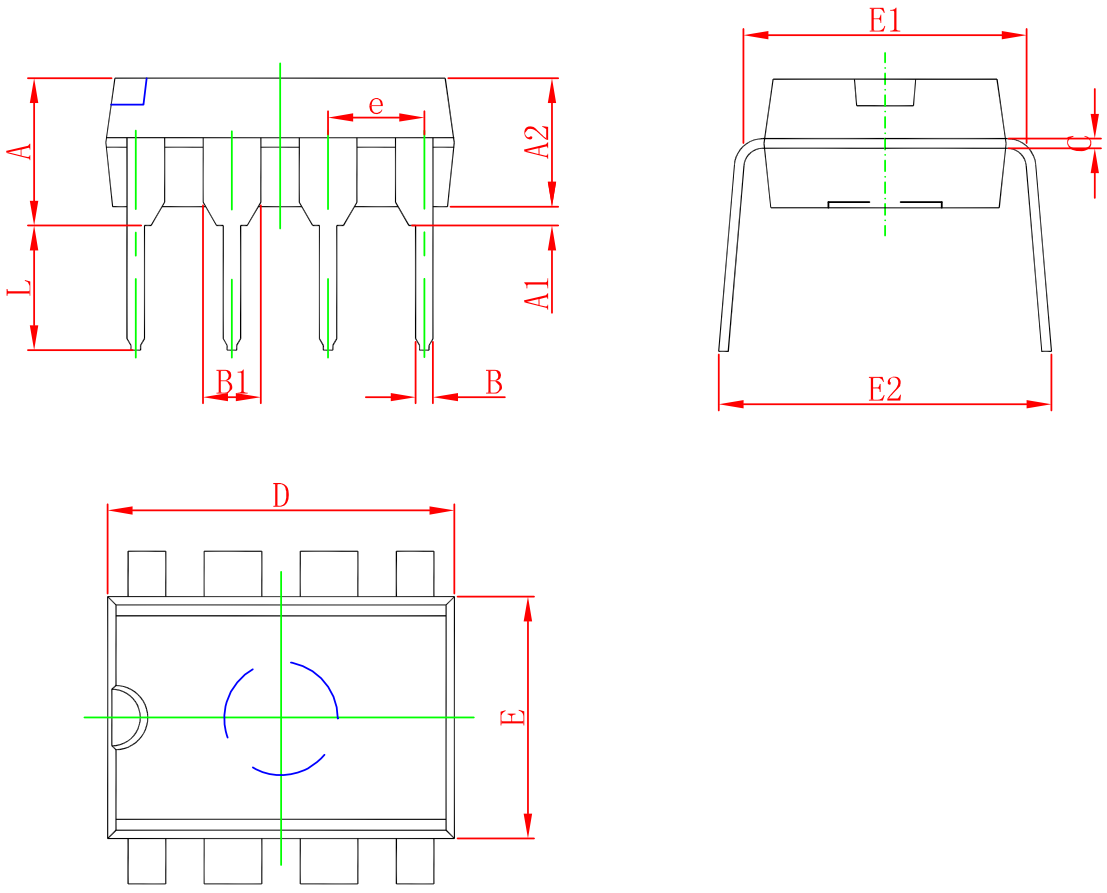
SOP8



SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCH	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGE INFORMATION

DIP8



SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.26
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354